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DESIGN AND SIMULATION OF CASCADED SEVEN LEVEL H-BRIDGE MULTILEVEL INVERTER BASED DSTATCOM FOR POWER QYALITY IMPROVEMENT

Prof. Suryakant H. Pawar[*1] and Chetan A. Jambhulkar[2]

[*1]Associate Professor, Department of Electrical Engineering, Government College of Engineering, Karad, Maharashtra, India

[2]P. G. Student, Department of Electrical Engineering, Government College of Engineering, Karad, Maharashtra, India

ABSTRACT

In this paper the design of a DSTATCOM employing a Seven–Level Cascaded H-Bridge Multilevel Inverter (CHBMLI) in medium voltage distribution power system is presented. The DSTATCOM helps to improve sending end & receiving end voltage and current drawn from a Non Linear Load (NLL). The control strategy based on Synchronous Reference Frame (SRF) theory is designed so that the voltage injected by active filter is able to mitigate the voltage sag, imbalance in the source voltage and reduce the harmonic content. The Level Shifted PWM (LSPWM) techniques are adopted to investigate the performance of CHB inverter. The performance of the proposed DSTATCOM is validated through simulation using MATLAB software with its SIMULINK and Power System block set tool and also performance of the system without DSTATCOM and with DSTATCOM is evaluated.

Keywords— *DSTATCOM, Level Shifted Pulse Width Modulation (LSPWM), Cascaded H-Bridge Multilevel Inverter (CHBMLI), MOSFET.*

I. INTRODUCTION

In recent years Electrical Power Quality had obtained more attention in power engineering. In present day's power distribution systems is suffering from severe power quality problems. These power quality problems include high reactive power burden, harmonics currents, load unbalance, excessive neutral current etc. The measure of power quality depends upon the needs of the equipment that is being supplied. Usually the term power quality refers to maintaining a sinusoidal waveform of bus voltages at rated voltage and frequency [1]. The waveform of electric power at generation stage is purely sinusoidal and free from any distortion. Many of the Power conversion and consumption equipment are also designed to function under pure sinusoidal voltage waveforms. However, there are many devices that distort the waveform. These distortions may propagate all over the electrical network. In recent years, there has been an increased use of non-linear loads which has resulted in an increased fraction of non-sinusoidal currents and voltages in Electric Network. The wave shape phenomena associated with power quality may be characterized into synchronous and non synchronous phenomena. Synchronous phenomena refer to those in synchronism with A.C waveform at power frequency [10], [13].

A group of controllers together called Custom Power Devices (CPD), which include the DSTATCOM (distribution static compensator), The DSTATCOM, is a shunt-connected device, which takes care of the power quality problems in the currents it consists of a dc capacitor, three-phase inverter (IGBT, MOSFET) module, ac filter, coupling transformer and a control strategy. The basic electronic block of the D-STATCOM is the voltage-sourced inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency. The D-STACOM employs an inverter to convert the DC link voltage Vdc on the capacitor to a voltage source of adjustable magnitude and phase. Therefore the D-STATCOM can be treated as a voltage controlled source. The D-STATCOM can also be seen as a current-controlled source. The DSTATCOM is based on the instantaneous real-power theory; it provides good compensation characteristics in steady state as well as transient states [9]. The instantaneous real-power theory generates the reference currents required to compensate the distorted line current harmonics and reactive power. It also tries to maintain the dc-bus voltage across the capacitor constant.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor [5], [6], [8], [11]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. This paper presents a DSTATCOM with a proportional integral controller based CHB multilevel (seven level) inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

II. DISTRIBUTED STATIC SYNCHRONOUS COMPENSATOR (DSTATCOM)

A. Basic Configuration of DSTATCOM

The DSTATCOM is a voltage or current source inverter based custom power device connected in shunt with the power system. It is connected near the load at the distribution systems [12], [14]. The basic structure of DSTATCOM is presented in Figure 2.1 As shown in Figure 2.1; DSTATCOM consists of an inverter, dc link capacitance *C* that providing the dc voltage for inverter, coupling inductance *L* used for current filter and reactive power exchange between DSTATCOM and power system and a control unit to generate PWM signals for the switches of inverter. In Figure 4, and *R* respectively represent switching losses in inverter and winding resistance of coupling inductance [6].

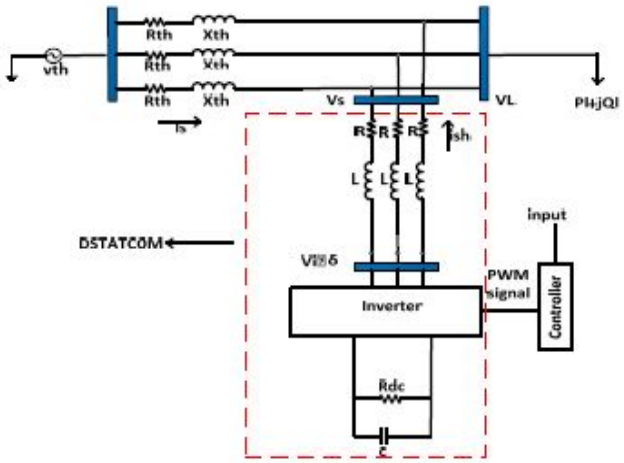

Figure 2.1 - Basic structure of DSTATCOM in distribution system

B. Cascaded H-Bridge Inverter Topologies

The N-level cascaded H-bridge, multilevel inverter comprises series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source. Figure 2.2 shows one phase of an n-level cascaded H-bridge inverter. The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches. Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.

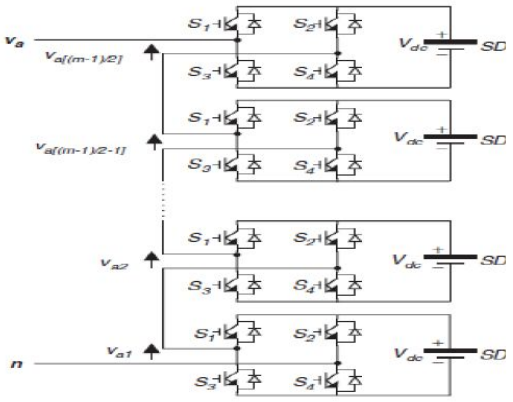

Figure 2.2 - Single-Phase Structure of a Multilevel Cascaded H-Bridge Inverter

• The number of levels in the line-to-line voltage waveform will be k= 2N-1,

• While the number of levels in the line to neutral of a star (wye) load will be p = 2k −1

• The number of capacitors or isolated supplies required per phase is Ncap = ½(N −1)

• The number of possible switch states is nstates = N phases

• The number of switches in each leg is Sn = 2(N −1)

Figure 2.3 shows the seven level multilevel inverter and. Here even though we have twelve switches at any switching state only two switches are on/off at a voltage level of Vdc/3, so switching losses are reduced. In three level inverter dv/dt is Vdc, but in five level inverter dv/dt is Vdc/2 and in seven level inverter dv/dt is Vdc/3. As dv/dt reduces, the stress on switches reduces and EMI also reduces.

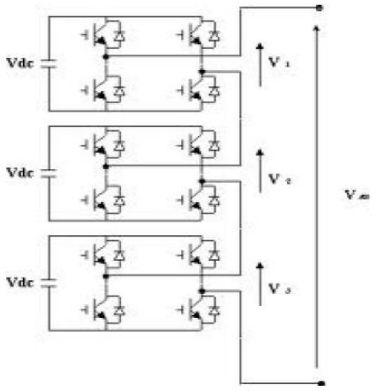

Figure 2.3 - Block diagram of 7-level CHB inverter model

III. REFERENCE CURRENT CONTROL STRATEGY

The control scheme of the shunt active power filter must calculate the current reference signals from each phase of the inverter using instantaneous real-power compensator. The block diagram as shown in Figure 3, that control scheme generates the reference current required to compensate the load current harmonics and reactive power. The PI controller is tried to maintain the dc-bus voltage across the capacitor constant of the cascaded inverter. This instantaneous real- power compensator with PI-controller is used to extracts reference value of current to be compensated.

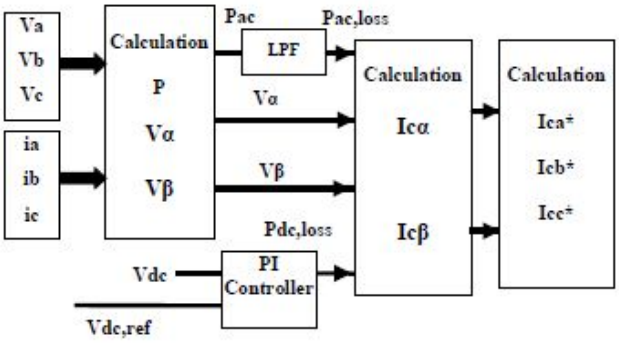

Figure 3: Reference current generator using instantaneous real-power theory

These reference currents isa*, isb *and isc * are calculated instantaneously without any time delay by using the instantaneous α,β coordinate currents. The required references current derivate from the inverse Clarke transformation and it can be written as

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3/2} \\ -1/2 & -\sqrt{3/2} \end{bmatrix} \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix}$$

The p-q theory performs a Clarke transformation of a stationary system of coordinates a b c to an orthogonal reference system of coordinates α,β . In a b c coordinates axes are fixed on the same plane, apart from each other by 120 that as shown in Fig 5. The instantaneous space vectors voltage and current Va , ia are set on the a axis, Vb , ib are on the b axis, and Vc , ic are on the c axis. These space vectors are easily transformed into α,β coordinates. The instantaneous source voltages vsa, vsb, vsc are transformed into α, β coordinate's voltage by Clarke transformation as follows:

$$v_{\alpha\beta 0} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} v_{abc}$$

Similarly, the instantaneous source current isa, isb, isc also transformed into α, β coordinate's current by Clarke transformation that is given as

$$i_{\alpha\beta 0} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} i_{abc}$$

Where α and β axes are the orthogonal coordinates. They Vα, iα are on the α-axis, and Vβ, iβ are on the β-axis. The reference currents isa*, isb * and isc * are compared with actual source current isa , isb and isc that facilitates generating cascaded multilevel inverter switching signals using the proposed triangular-sampling current modulator. The small amount of real-power is adjusted by changing the amplitude of fundamental component of reference currents and the objective of this algorithm is to compensate all undesirable components. When the power system voltages are balanced and sinusoidal, it leads to constant power at the dc bus capacitor and balanced sinusoidal currents at AC mains simultaneously.

IV. PWM TECHNIQUES FOR CHB INVERTER

The most popular PWM techniques for CHB inverter are 1.Phase Shifted Carrier PWM (PSCPWM), 2.Level Shifted Carrier PWM (LSCPWM).

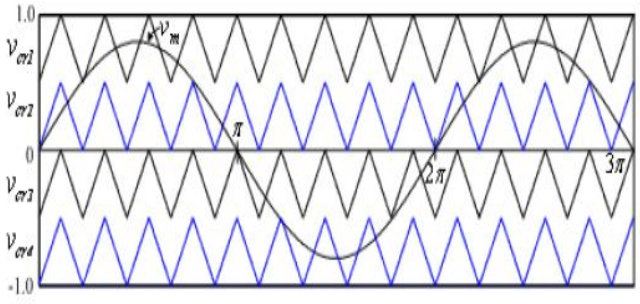

Figure 4: Level Shifted Carrier PWM (LSCPWM)

Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier level shifted by 1/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

V. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Figure 5.1 and 5.6 shows the MATLAB/SIMULINK power circuit model of DSTATCOM. It consists of four blocks named as source block, nonlinear load block, control block, measurement block. The system parameters for simulation study are source voltage of 11 KV, 50 Hz AC supply, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mH. Load resistance and inductance are chosen as 60ohm and 30 mH respectively.

A) Without compensation

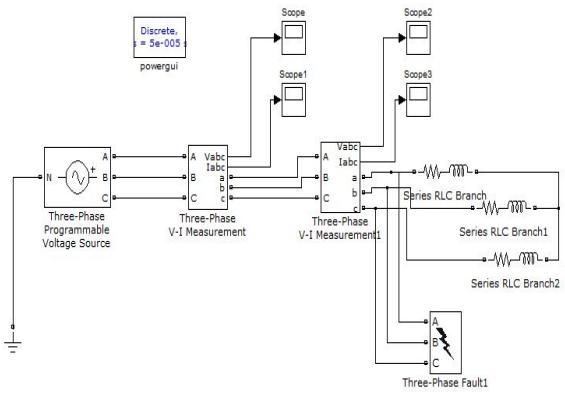

Fig.5.1 SIMULINK model without DSTATCOM

In this model a three phase source of 11 KV is connected to non linear load. When this is connected to the source a dip in voltage called sag occurs. Due to the sag the voltage will get increased. Without compensation means no compensating device is connected to compensate the voltage sag. This dip in voltage is the pollution caused by the non linear loads.

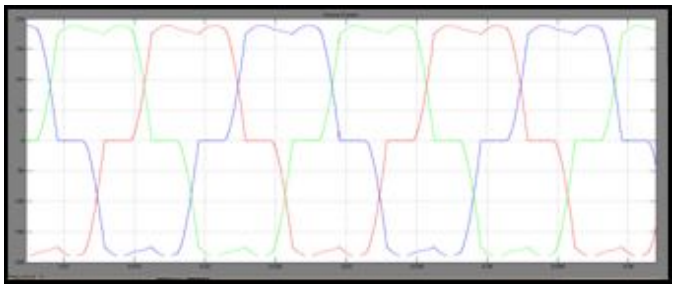

Figure 5.2: Source Current without DSTATCOM

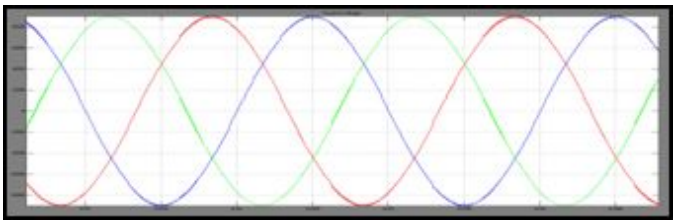

Figure 5.3: Source Voltage without DSTATCOM

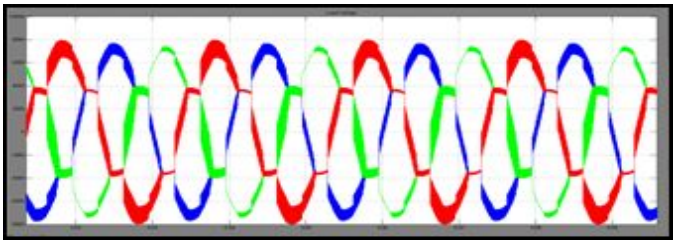

Figure 5.4: Load Current without DSTATCOM

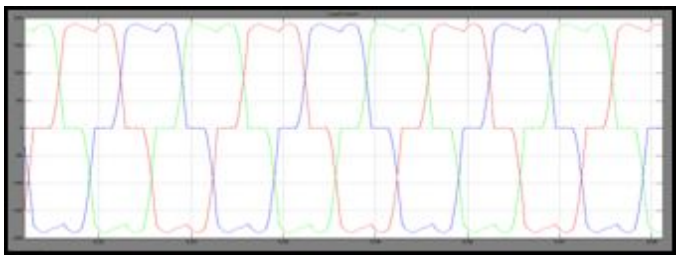

Figure 5.5: Load Current without DSTATCOM

B) With compensation

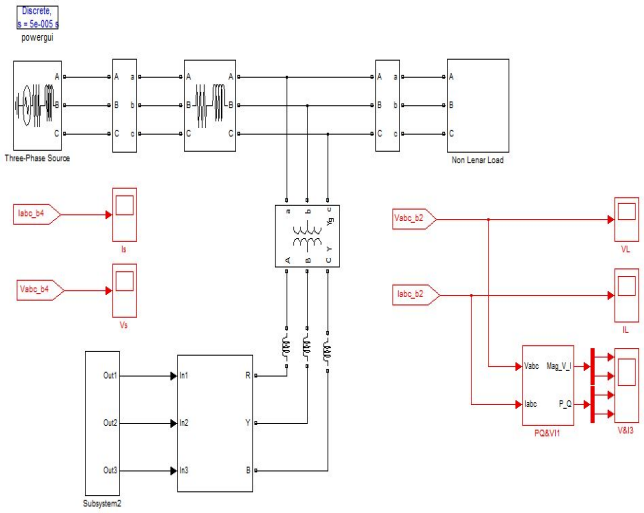

Fig.5.6 SIMULINK model with DSTATCOM

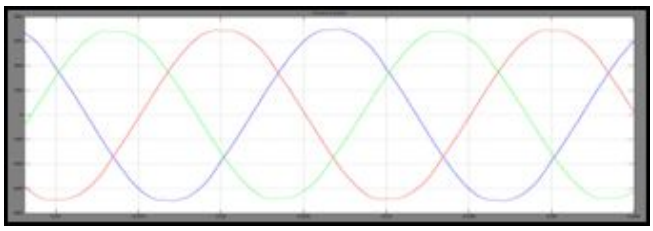

Figure 5.7: Source Current with DSTATCOM

Figure 5.8: Source Voltage with DSTATCOM

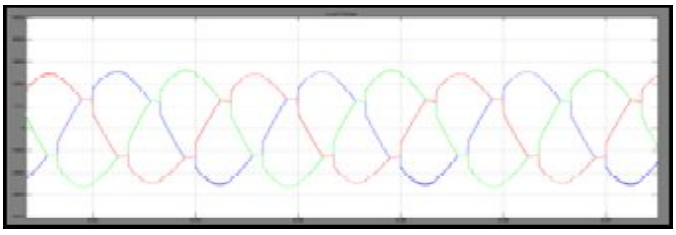

Figure 5.9: Load Current without DSTATCOM

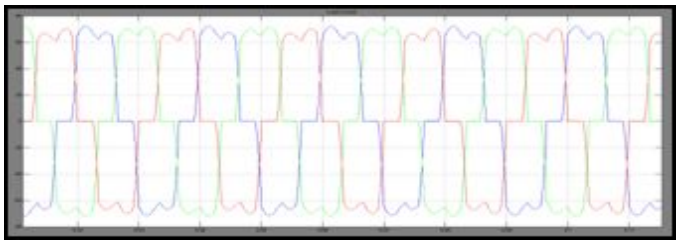

Figure 5.10: Load Current with DSTATCOM

VI. CONCLUSION

A model of system feeding nonlinear loads has been developed using MATLAB SIMULINK. DSTATCOM with Cascaded H-bridge Inverter is investigated. The cascaded H-bridge multilevel boost inverter without inductors uses a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg. The load voltage, RMS

Voltage, current, real power, reactive power under nonlinear loads is simulated. From the results it is seen that there is an improvement in power factor. Finally, the performance of the system without DSTATCOM and with DSTATCOM using CHB is evaluated**.**

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