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# DESIGN OF SUBTHRESHOLD ADIABATIC LOGIC FOR LOW POWER AND LOW LEAKAGE CIRCUITS

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**ABSTRACT** The demand for implementing ultralow-power digital systems in many modern applications, such as mobile systems, sensor networks, and implanted biomedical systems, has increased the importance of designing logic circuits in sub threshold regime In sub threshold logic, circuits operate with a supply voltage VDD lower than the transistor threshold voltage VT and utilize the sub threshold leakage current as the operating current. Behavior of adiabatic logic circuits in weak inversion or sub threshold regime is analyzed in depth for the first time in the literature to make great improvement in ultra low power circuit design. This novel approach is efficacious in low-speed operations where power consumption and longevity are the pivotal concerns instead of performance. Simulations output show that sub threshold adiabatic units can save significant energy compared with a logically equivalent static CMOS implementation.

## I. INTRODUCTION

Even those tiny micro power circuits need a source of power, and that source is a distinct, discrete component, of course - and often physically larger than the circuit it supplies. While energy harvesting may be a viable way to get the needed power, in many cases it may be unavailable, impractical, or too inefficient. Developers of battery-powered devices often have the challenge to offer high levels of functionality and performance while simultaneously maximizing battery life. Applications like water and gas flow meters, medical monitoring devices and remote sensors typically demand months or even years of battery life from a single battery. In some cases, developers are also challenged to develop next generation products with no battery at all, requiring energy harvesting from environmental sources such as heat, vibration and light. Furthermore, as the demand for longer battery life and smaller batteries increases in more applications, users continue to demand more functionality and higher performance in their products. To maximize functionality and battery life, developers of these battery-powered applications must consider many factors in their system architecture and design. In these applications, the microcontroller is a primary power consumer and developers must carefully consider the way energy is used. This article focuses on breaking down the primary modes in which microcontrollers consume energy by describing the critical parameters that must be considered in each of these modes, and by providing a holistic framework for developers to evaluate and compare microcontrollers in the context of specific applications. By understanding the many ways microcontrollers consume energy, developers can make system architecture decisions, choose optimal components and provide microcontroller users with optimized functionality and longer battery life.

## II. METHODOLOGY

**Adiabatic logic:** Recently, adiabatic logic (or energy recovery logic) style has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability. These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime. Since the performance requirements are quite relaxed in many of these energy efficient Sub threshold applications, we believe that the adiabatic style can be used efficaciously in a sub threshold regime to make the circuit more energy efficient. To the best of our knowledge, no paper emphasizes the application of adiabatic logic in weak inversion regime for advanced technology node such as 22 nm. Therefore, the attempt to realize the sub threshold adiabatic logic (SAL) concept is a new endeavor

In many applications ultra low Power based circuit design has become a primary design metric for manufactures. Due to technological advancement, power reduction is highest in jurisdiction when compared to speed and performance. Higher Power consumption increases the on-chip temperature which results in reduced operating life of the chip and battery life . To satisfy the low power requirement of the CMOS based circuits, sub-threshold adiabatic logic is being introduced which involves scaling

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voltage below the device threshold . Extensive research is going on the subjects of sub/near-threshold digital design and their challenges, the goal of this paper however is to cover a border range of subthreshold based digital system designs, to show the interrelation of different solutions and their effective methods for low power digital design and review the recent updates and new advances in ultra low power era .

## III. CHALLENGES IN SUBTHRESHOLD DESIGN

Impediment: The first and preeminent challenges of the circuit operation in the subthreshold region is the longer impediment or delay relatively having lower frequency due to weak current flow in the channel. Device scaling: The device scaling provides great merits like reduction in gate capacitance, switching energy and gate delay. On the other hand there are some demerits like including process variability, increased subthreshold leakage, increased gate leakage at super-threshold voltages, Exponential sensitivities to Vth, Vdd, and inverse subthreshold slope. Exploring new logic families for robust design: The current ratio ION/IOFF decreases with low Vdd which may reduce robustness due to this reason static CMOS gates works continuous and gives better results in subthreshold but because of scaling, voltage or process variation and other arising effects CMOS offer greater resiliency.Temperature: The effect of temperature variation on the circuit behavior is an another important challenge, mobility degradation in the channel during strong inversion generally slow down the circuit and also rises the temperature. This arising temperature decreases threshold voltage which exponentially increases subthreshold current.Reliability problems: Reliability failures are typically caused by marginal manufacturing defects that are not significant enough to prevent the IC from passing a production test but can cause failure under use. Test coverage problems and circuit sensitivity are always followed by reliability problem. Reliability problems are worst kind of problems due to potentially severe consequences.

**Silicide/Salicide Technology**

Used to reduce interconnect resistivity by placing a low-resistance silicide such as TiSi2,WSi2, TaSi2, etc. on top of polysilicon Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.

## IV. EXISTING SYSTEM DESIGN

In existing method the negative feed back is flow in the circuit due to dynamic power consumption which caused the damage in the circuit and increase the power consumption

The power dissipation switching power, that may dissipation cannot be lowered than, this one by using this conventional static CMOS circuits

The demand for implementing ultralow-power digital systems in many modern applications, such as mobile systems, sensor networks, and implanted biomedical systems, has increased the importance of designing logic circuits in subthreshold regime.

**Drawback of conventional cmos logic**

Which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules:

Never turn on a when there is a voltage potential between the source and drain.

Never turn off a transistor when current is flowing through it.

## V. SOURCES OF POWER DISSIPATION

Power consumption is an important property of a design that affects feasibility cost and reliability. It influence a greater number of critical design decisions, such as power supply capacity, the battery lifetime, supply line sizing, packaging and cooling requirements. There are three major sources of power dissipation in digital CMOS circuits which are summarized in the following equation .

Pavg = Pswitching + Pshortcircuit + Pleakage

α0-1. CL · Vdd2 · fclk + Isc · Vdd + Ileakage · Vdd

**Leakage and Scaling**

**Leakage and scaling are directly related**

- constant field scaling would result in continued exponential increase in leakage
- n Vt would continue to be reduced, increasing Io f f
- Io f f = I( qVtmkT )

**Primary Leakage Problems**

- Overall power of a chip
- Stability of 6T SRAM cells
- Noise immunity of dynamic logic gates Sources

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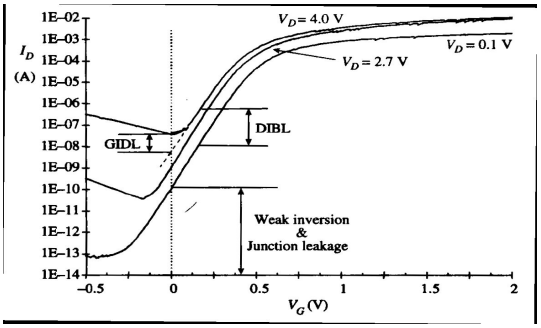
**Leakage Sources**




## VI. PROPOSED SYSTEM

Adiabatic logic (or energy recovery logic) style has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime.

subthreshold logic, circuits operate with a supply voltage VDD lower than the transistor threshold voltage VT and utilize the subthreshold leakage current as the operating current. Conventional CMOS logic circuits utilizing subthreshold

Transistors can typically operate with a very low power consumption, which is mainly due to the dynamic (switching) power consumption and is quadratically dependent upon the supply voltage as CL f V2 DD (where CL , f , and VDD are the load capacitance, operating frequency, and the supply voltage,respectively).

The demand for implementing ultralow-power digital Systems in many modern applications, such as mobile Systems, sensor networks, and implanted biomedical systems, Has increased the importance of designing logic circuits in Sub threshold regime. These emerging applications have low Energy as the primary concern instead of performance, with The eventual goal of harvesting energy from the environment In a proposed system we design the adiabatic logic with DTCMOS logic.

adiabatic logic circuits in weakinversion or subthreshold regime is analyzed in depth for the first time in the literature to make great improvement in ultra lowpower circuit design. This novel approach is efficacious in low-speed operations where power consumption and longevity are the pivotal concerns instead of performance.

**Principle of Adiabatic Switching**

Adiabatic switching is used to minimize energy losses during the charging/discharging cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. Here, the load capacitance (CL) is charged by using a constant current source (I) while in conventional CMOS logic we use constant voltage source to charge the load capacitance. Here R is the on-resistance of PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage zero initially

## VII. SOFTWARE DESCRIPTION

TANNER EDA:

Tanner EDA tools for analog and mixed-signal ICs and MEMS design offers designers a seamless, efficient path from design capture through verification. Our powerful, robust tool suite is ideal for applications including Power Management, Life Sciences / Biomedical, Displays, Image Sensors, Automotive, Aerospace, RF, Photovoltaics, Consumer Electronics and MEMS.

TANNER EDA INCLUDES:

- S-EDIT (SCHEMATIC EDIT)
- W-EDIT(WAVEFORM EDIT)
- T-SPICE
- T-SPICE:

Tanner T-Spice™ Circuit Simulator puts you in control of simulation jobs with an easy-to-use graphical interface and a faster, more intuitive design environment. With key features such as multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simpler SPICE syntax creation, T-Spice saves you time and money during the simulation phase of your design flow.

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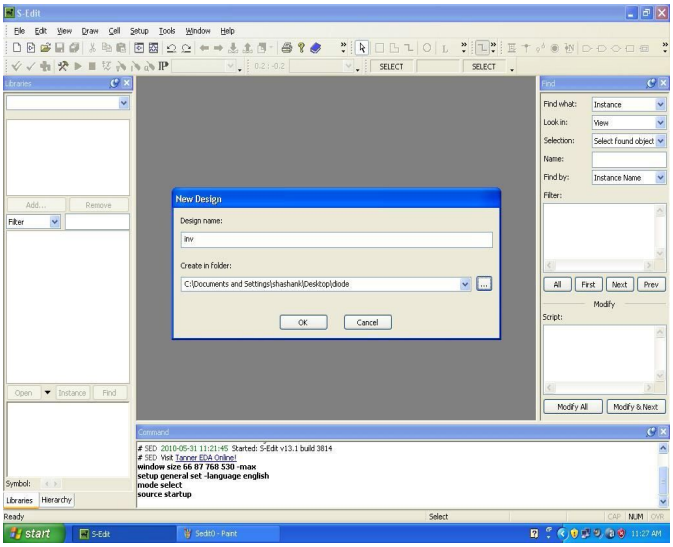
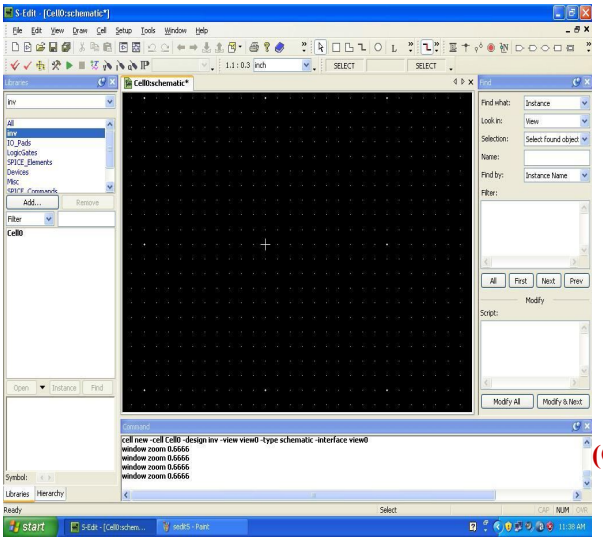
T-Spice enables more accurate simulations by supporting the latest transistor models—including BSIM4 and the Penn State Philips (PSP) model. Given that T-Spice is compatible with a wide range of design solutions and runs on Windows® and Linux® platforms, it fits easily and cost effectively into your current tool flow.

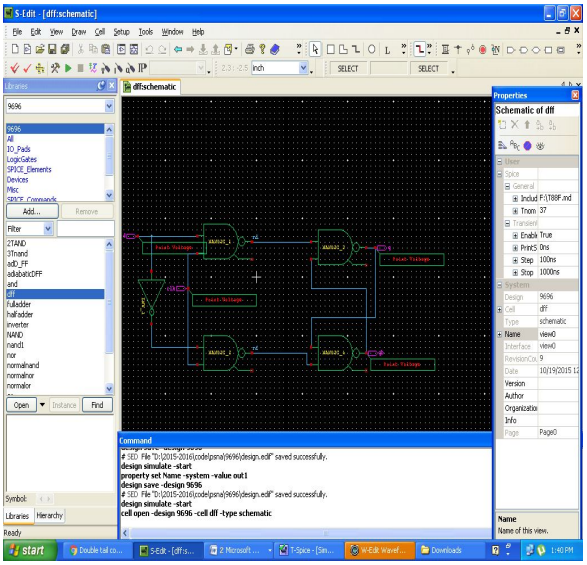
T-Spice provides extensive support of behavioral models using Verilog-A, expression controlled sources, and table-mode simulation. Behavioral models give you the flexibility to create customized models of virtually any device. T-Spice also supports the latest industry models, including the transistor model recently selected as the next standard for simulating future CMOS transistors manufactured at 65 nanometers and below—the Penn State Philips (PSP) model. PSP will simplify the exchange of chip design information and support more accurate digital, analog, and mixed-signal circuit behavior analysis.
T-Spice also supports foundry extensions, including HSPICE® foundry extensions to models.

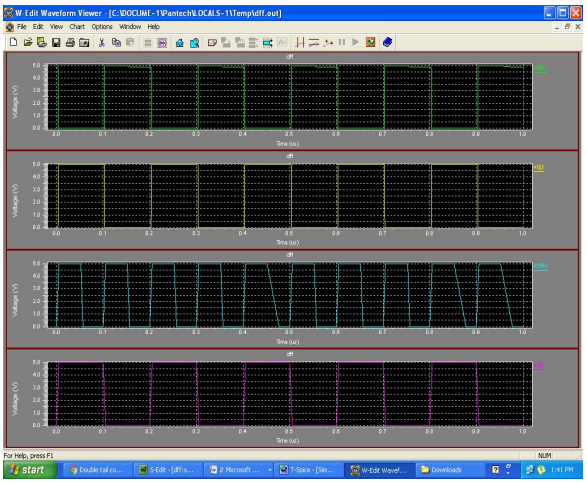



## VIII. EXISTING OUTPUT

### D flip flop




**Power Results**
vdd gnd from time 1e-008 to 1e-006
**Average power consumed** ->
4.798298e-003 watts
**Max power** 3.390615e-002 at time
9.03301e-007
**Min power** 1.897431e-003 at time
1e-007

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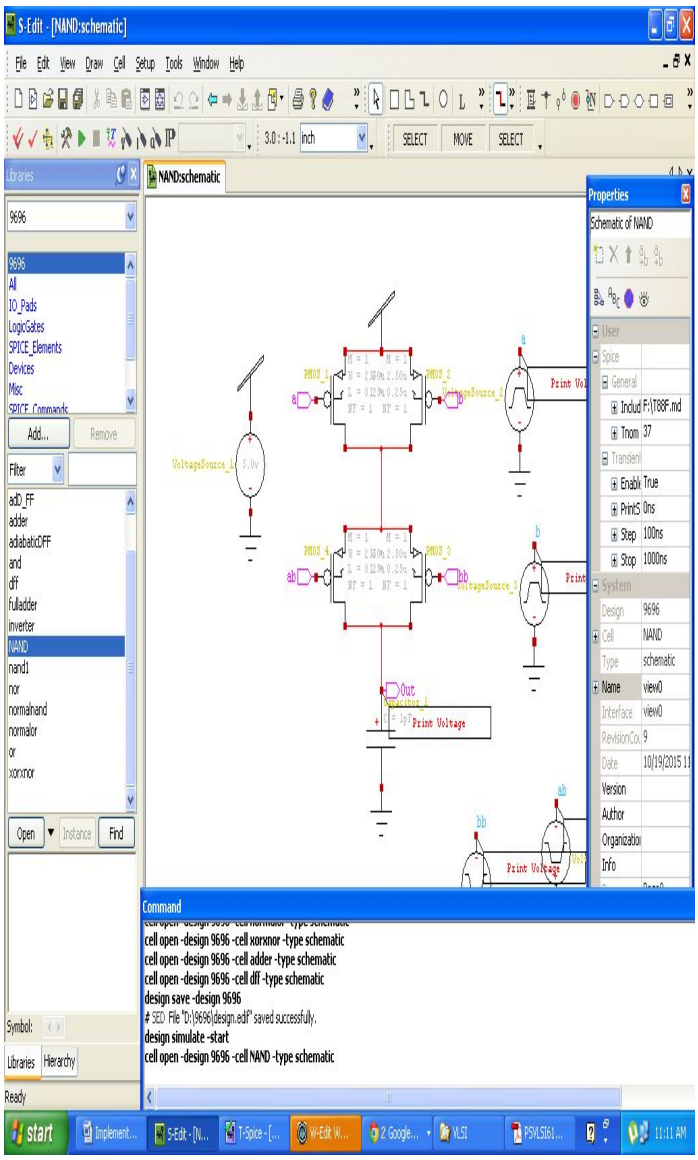
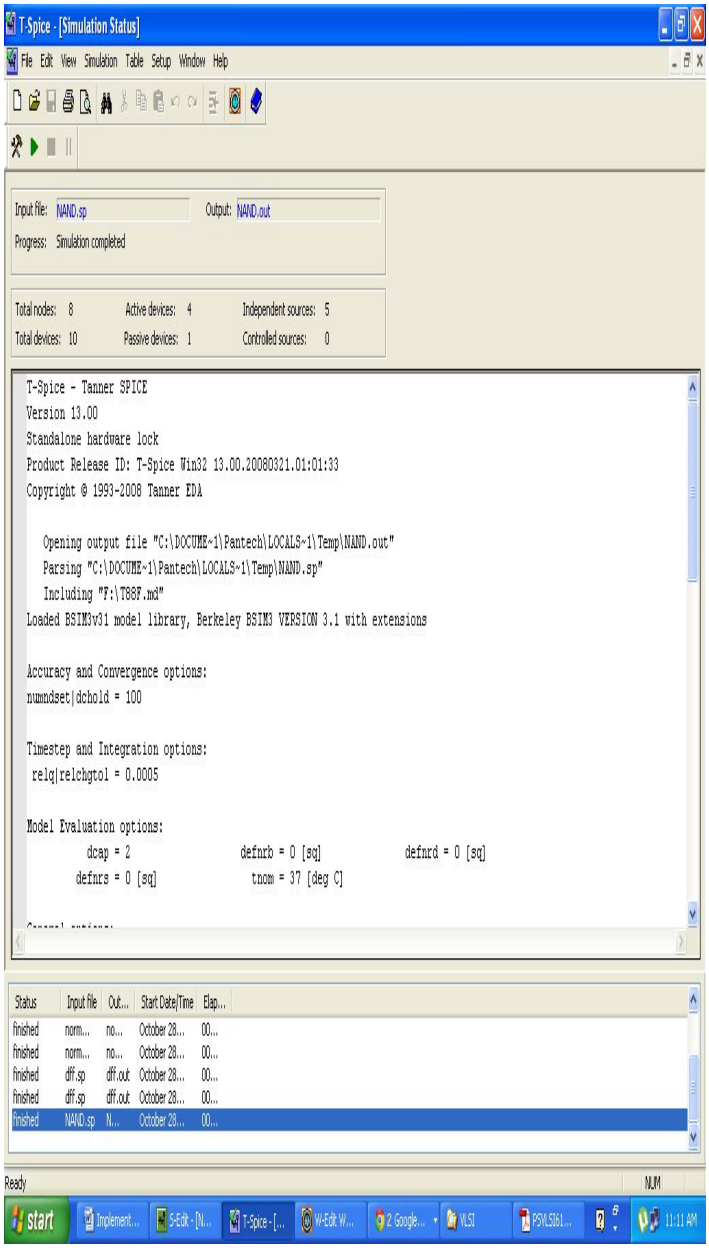
**PROPOSED OUTPUT:**

**ADIABATIC NAND GATE**




**Power consumption:**

Average power consumed -> 8.292000e-008 watts
Max power 1.383347e-005 at time 2.05e-007
Min power 2.562093e-013 at time 4.52e-007




## IX. CONCLUSION

SAL has been presented in this paper for the first time in the literature to advance the ultralow power research. A closedform expression of the energy dissipation has been derived, from which insight is gained into the dependence of energy dissipation on design and process parameters. SAL saves considerable energy compared with the static

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conventional logic counterpart over a wide range of frequency. In particular, the impact of temperature variation on leakage dissipation, output swing, etc., has been discussed thoroughly in this paper. Hence, the predicted values of optimum frequency and optimum supply voltage almost match the simulated ones. Post layout simulations using CADENCE SPICE Spectra and the comparison with the static counterpart explain the workability of SAL. This proposed logic scheme can be used in future energy-saving embedded circuits and mainly for energy efficient devices where ultralow power and longevity are the pivotal issues.

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